Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

ATTY DOCKET NO.	SERIAL NO.
247561US2	10/754,539
APPLICANT: Takuji MATSUMOTO, et al.	
FILING DATE: January 12, 2004	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
ah	AO	10-209167	08/07/1998	JAPAN (with English extract)		
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

ah	AW	Y. HIRANO, et al., IEEE International SOI Conference, pages 131-132, "BULK-LAYOUT-COMPATIBLE 0.18μm SOI-CMOS TECHNOLOGY USING BODY-FIXED PARTIAL TRENCH ISOLATION (PTI)", October 1999
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ah	AY	Y. HIRANO, et al., IEEE, IEDM, pages 467-470, "IMPACT OF 0.10 μm SOI CMOS WITH BODY-TIED HYBRID TRENCH ISOLATION STRUCTURE TO BREAK THROUGH THE SCALING CRISIS OF SILICON TECHNOLOGY", 2000
ah	AZ	S. MAEDA, et al., Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, pages 270-271, "A HIGHLY RELIABLE 0.18 μm SOI CMOS TECHNOLOGY FOR 3.3V/1.8V OPERATION USING HYBRID TRENCH ISOLATION AND DUAL GATE OXIDE", 2001

☐ Additional References sheet(s) attached

Examiner: Andrew Kim Date Considered: 05/03/05

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.